

IN THE SPECIFICATION:

Please replace the paragraph at page 5, line 18, with the following replacement paragraph:

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A2  
Figure 3 is a diagram illustrating the disabling of learning by the switching module 25 of data packets transferred between the router interface port 20d and the router 16 according to an embodiment of the present invention. As described above, the host CPU 26 is configured for controlling the network switch 12: each of the network switch ports 20 has a corresponding learning bit which, when set, causes the switch fabric 25 to learn layer 2 and layer 3 addresses of the data packets received by the corresponding switch port 20. Hence, the host CPU 26 begins in step 40 by setting the learning bit on all the ports to "1". The host CPU 26 then identifies the router interface port 20d that is configured for sending and receiving data packets to the router 16 in step 42. The host CPU 26 then disables (i.e., it resets) the learning bit to zero on the router interface port in step 44. After the learning bit has been disabled on the router interface port 20d, the network switch 12 is ready to begin switching data packets.

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